

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	94	703/14.ccls. and @pd>"20061201"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/05/03 14:14

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L4	13	(bidirectional adj node) and simulat\$4	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/05/03 14:16
L5	12	biput	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/05/03 14:18
L6	2	(((mixed near signal) or mixed-signal) near simulation) and @pd>"20061201"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/05/03 14:19
L7	1	(((analog near digital) or analog-digital or digital-analog) near simulation) and @pd>"20061201"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/05/03 14:19



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[Voltage level translation for an output driver system with a bias generator - group of 2 »](#)

F Hinedi, M Cases, S Dutta, RH Dennard - US Patent 5,986,472, 1999 - Google Patents
... A gate of transistor 118 is connected to bias circuit 130 at Node E. A drain of transistor 118 is connected to an information node **IOPUT**, which is connected to ...

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[Stacked PFET off-chip driver with a latch bias generator for overvoltage protection - group of 3 »](#)

F Hinedi, L Mamileti - US Patent 6,141,200, 2000 - Google Patents

... GND **IOPUT** Page 2. ... multiply/add operations, and includes floatingpoint registers output terminal **IOPUT**. 120 performs single precision and/or double precision ...

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[Discrete adaptive control: A sufficient condition for stability and applications - group of 3 »](#)

JJ Fuchs - Automatic Control, IEEE Transactions on, 1980 - [ieeexplore.ieee.org](#)

... we-**ioput** singleoutput systems is considered using a model-reference type approach. A sufficient condition upon the adaptation mechanism is obtained Any ...

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[Concurrent Hierarchical and Multilevel Simulation of VLSI Circuits - group of 3 »](#)

RB Mueller-Thuns, JT Rahmeh, JA Abraham, JA Wehbeh ... - SIMULATION, 1993 - [intl-sim.sagepub.com](#)

Page 1. 79 TECHNICAL ARTICLE Concurrent Hierarchical and Multilevel Simulation of VLSI Circuits & dagger; Robert B. Mueller-Thuns Cadence Design System Inc. ...

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[Circuit and method for voltage level translation utilizing a bias generator - group of 2 »](#)

F Hinedi, M Cases, S Dutta, RH Dennard - US Patent 5,867,010, 1999 - Google Patents
... the art. Resistor 110 couples clamp device 102 to an external signalling device via signal pad input, **IOPUT**, 112. Diode devices ...

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[The de Bruijn multiprocessor network: a versatile parallel processing and sorting network for VLSI - group of 9 »](#)

MR Samatham, DK Pradhan - IEEE Transactions on Computers, 1989 - [doi.ieeecomputersociety.org](#)

... input/sequential output, 2) parallel input/sequential output, 3) parallel input/parallel output, 4) sequential input/parallel output, 5) hybrid **ioput**/l@rid ...

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IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

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- 2. On-Line Simulation of Block-Diagram Systems
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